TSQS-854HG01-MC Optical Transceiver

Multi-mode 400G-SR8 QSFP-DD Transceiver, With Diagnostic Monitoring
8 channels full-duplex 100m Transceiver

Features

- Hot-pluggable QSFP-DD form factor
- Power dissipation < 10W
- Maximum link length of 100m on OM4 fiber with KP4 FEC
- 8x50Gb/s PAM4 VCSEL transmitter
- 8x50G PAM4 retimed 400GUAI-8 electrical interface aligned with IEEE 802.3bs
- I2C management interface
- MPO-16 APC connector
- Operating case temperature: 0°C~+70°C
- RoHS6 compliant (lead free)

Applications

- 400G 100m on OM4 with FEC

Description

The TSQS-852HG01-MC QSFP-DD SR8 transceiver modules are designed for use in Gigabit Ethernet links on up to 70m on OM3 MMF or 100m on OM4 MMF. They are compliant with the QSFP-DD MSA and portions of IEEE P802.3bs. Digital diagnostic functions are available via the I2C interface, as defined by the CMIS 4.0.

Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Parameters	Symbol	Min.	Max.	Unit
Power Supply Voltage	VCC	-0.5	+3.6	V
Storage Temperature	Tc	-40	+85	°C
Relative Humidity[1]	RH	15	85	%

Notes:
[1] Non-condensing.

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Recommended Operating Environment

Parameter	Symbol	Min	Typical	Max	Unit
Power Supply Voltage	VCC	3.15	3.30	3.45	V
Supply current	Icc	-	-	2898	mA
Operating Case Temperature	Tca	0	-	70	°C

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit
Transmitter					
Signaling rate per lane	-	26.5625± 100 ppm			GBd
Differential peak-peak input voltage tolerance[1]	Vin	900	-	-	mV
Differential input return loss	-	Per equation (83E–5) IEEE802.3bm			-
Differential to common mode input return loss	-	Per equation (83E–6) IEEE802.3bm			-
Differential termination mismatch	-	-	-	10	%
Module stress input test[2]	-	Per 120E.3.4.1 IEEE802.3bs			-
Single-ended voltage tolerance range	-	-0.4	-	3.3	V
DC common mode voltage[3]	-	-350	-	2850	mV
Receiver					
Signaling rate per lane	-	26.5625± 100 ppm			GBd
AC common-mode output voltage (RMS)	-	-	-	17.5	mV
Differential peak-to-peak output voltage	-	-	-	900	mV
Near-end ESMW (Eye symmetry mask width)	-	0.265			UI
Near-end Eye height, differential (min)	-	70	-	-	mV
Far-end ESMW (Eye symmetry mask width)	-	0.2			UI
Far-end Eye height, differential (min)	-	30	-	-	mV
Differential output return loss	-	Per equation 83E-2 IEEE802.3bm			-
Common to differential mode conversion return loss	-	Per equation 83E-3 IEEE802.3bm			-
Differential termination mismatch	-	-	-	10	%
Transition time (min, 20% to 80%)	-	9.5	-	-	ps
DC common mode voltage[3]	-	-350	-	2850	mV

Notes:

[1] With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

[2] Meets specified BER

[3] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

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Transmitter Specifications – Optical

Parameter	Symbol	Min	Typical	Max	Unit
Signaling Speed per Lane[1]	-	26.5625 ± 100ppm			GBd
Modulation format	-	PAM4			-
Center Wavelength	λ	840	850	860	nm
RMS spectral width[1]	Δλ	-	-	0.6	nm
Average Launch Power per Lane	Po	-6.5	-	4	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane[2]	OMA	-4.5	-	3	dBm
Launch power in OMAouter minus TDECQ, each lane	-	-5.9	-	-	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	-	-	-	4.5	dB
TDECQ – 10log10(Ceq), each lane[3]	-	-	-	4.5	dB
Extinction Ratio	ER	3	-	-	dB
Optical Return Loss Tolerance	ORL	-	-	12	dB
Encircled Flux[4]	FLX	> 86% at 19 um < 30% at 4.5 um			-
Average launch power of OFF transmitter, each lane	-	-	-	-30	dBm

Notes:

[1] RMS spectral width is the standard deviation of the spectrum.

[2] Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value.

[3] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

[4] If measured into type A1a.2 or type A1a.3, or A1a.4, 50μm fiber, in accordance with IEC 61280-1-4.

Receiver Specifications – Optical

Parameter	Symbol	Min	Typical	Max	Unit
Signaling Rate per Channel	DR	26. 5625 ± 100ppm			GBd
Modulation format	-	PAM4			-
Center Wavelength	λ	840	850	860	nm
Damage Threshold[1]	DT	5			dBm
Average receive power, each lane[2]	RXPOW	-8.4	-	4	dbm
Receive power (OMAouter), each lane	RxOMA	-	-	3	dBm
Stressed Receiver Sensitivity (OMA) per Lane[3]	SRS	-	-	-3.4	dBm
Stressed eye closure for PAM4 (SECQ), lane under test[4]	-	4.5			dB
SECQ – 10log10(Ceq)f, each lane (max)[4]	-	4.5			dB
OMAouter of each aggressor lane	-	3			dBm
LOS De-Assert	Lda	-	-	-9	dBm

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LOS Assert	Lsa	-30	-	-	dBm
LOS Hysteresis	Lh	0.5	-	-	dB

Notes:

[1] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

[2] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

[3] Measured with conformance test signal at TP3 (see IEEE 802.3cd 138.8.10) for the BER specified in 138.1.1.

[4] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Bit Rate (all wavelengths combined)[1]	BR	-	-	425	Gb/s
Bit Error Ratio (pre-FEC)[2]	BER	-	-	2.4E-4	-
Maximum Supported Distances					
Fiber Type	-	-	-	-	-
OM3 MMF	LMAX1	-	-	70	m
OM4 MMF	LMAX2	-	-	100	m

Notes:

[1] Supports 400GBASE-SR8 per IEEE P802.3cm.

[2] As defined by IEEE P802.3cm.

QSFP-DD Transceiver Electrical Pad Layout

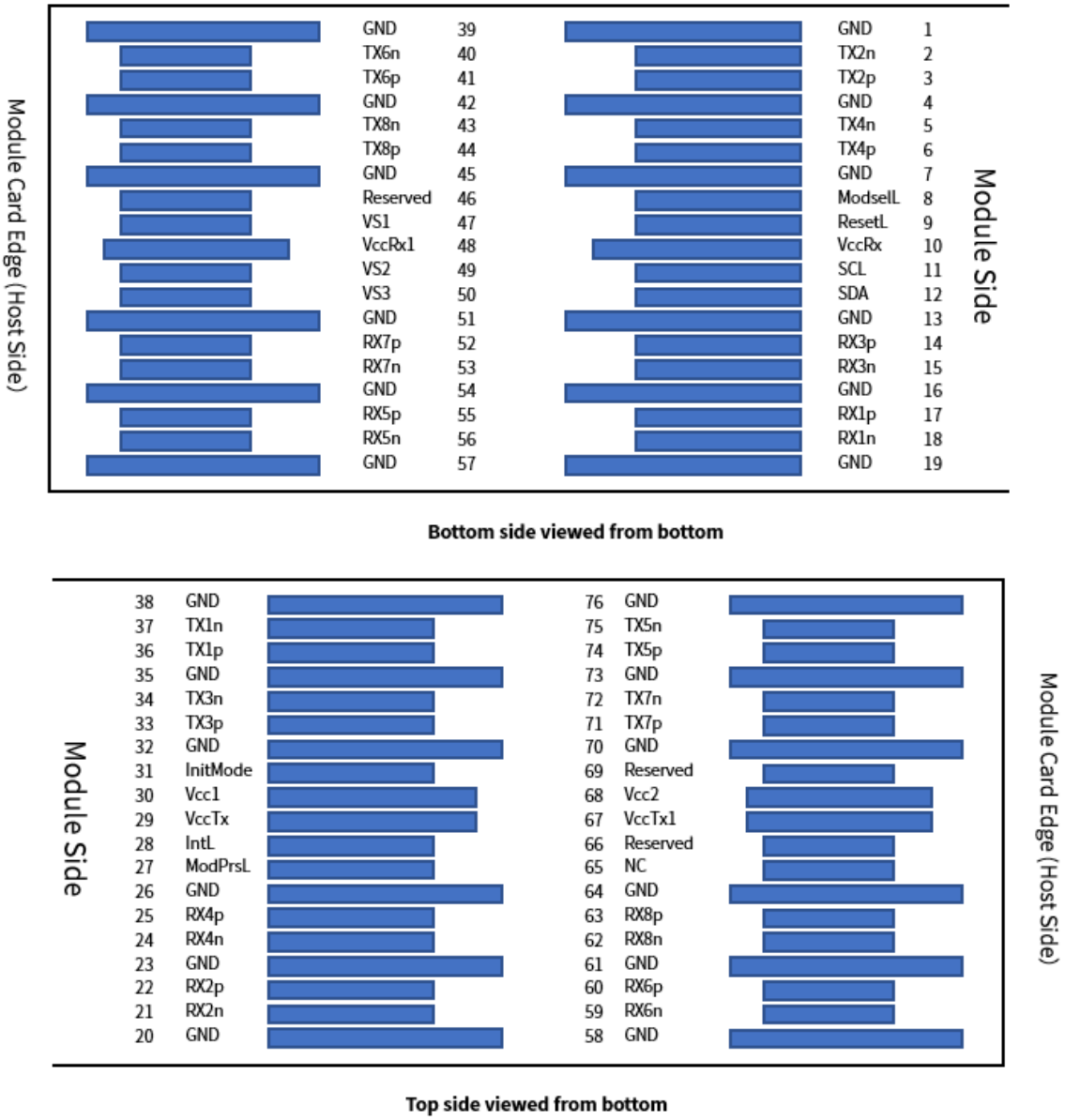

Figure 1 – QSFP-DD-compliant 76-pin connector (per QSFP-DD MSA)

Pin Definition

Pin	Symbol	Name/Description
1	GND	Module Ground
2	Tx2-	Transmitter inverted data input
3	Tx2+	Transmitter non-inverted data input
4	GND	Module Ground
5	Tx4-	Transmitter inverted data input

6	Tx4+	Transmitter non-inverted data input
7	GND	Module Ground
8	MODSEIL	Module Select
9	ResetL	Module Reset
10	VCCRx	+3.3V Receiver Power Supply
11	SCL	2-wire Serial interface clock
12	sda	2-wire Serial interface data
13	GND	Module Ground
14	RX3+	Receiver non-inverted data output
15	RX3-	Receiver inverted data output
16	GND	Module Ground
17	RX1+	Receiver non-inverted data output
18	RX1-	Receiver inverted data output
19	GND	Module Ground
20	GND	Module Ground
21	RX2-	Receiver inverted data output
22	RX2+	Receiver inverted data output
23	GND	Module Ground
24	RX4-	Receiver inverted data output
25	RX4+	Receiver non-inverted data output
26	GND	Module Ground
27	ModPrsL	Module Present, internal pulled down to GND
28	IntL	Interrupt output, should be pulled up on host board
29	VCCTx	+3.3V Transmitter Power Supply
30	VCC1	+3.3V Power Supply
31	InitMode	Initiallzation mode; In legacy QSFP applications, the InitMode pad is
32	GND	Module Ground
33	Tx3+	Transmitter non-inverted data input
34	Tx3-	Transmitter inverted data input
35	GND	Module Ground
36	Tx1+	Transmitter non-inverted data input
37	Tx1-	Transmitter inverted data input
38	GND	Module Ground
39	GND	Module Ground

40	Tx6-	Transmitter inverted data input
41	Tx6+	Transmitter non-inverted data input
42	GND	Module Ground
43	Tx8-	Transmitter inverted data input
44	Tx8+	Transmitter non-inverted data input
45	GND	Module Ground
46	Reserved	For future use
47	VS1	Module Vender Specific 1
48	VCCRx1	+3.3V Power Supply
49	VS2	Module Vender Specific 2
50	VS3	Module Vender Specific 3
51	GND	Module Ground
52	RX7+	Receiver non-inverted data output
53	RX7-	Receiver inverted data output
54	GND	Module Ground
55	RX5+	Receiver non-inverted data output
56	RX5-	Receiver inverted data output
57	GND	Module Ground
58	GND	Module Ground
59	RX6-	Receiver inverted data output
60	RX6+	Receiver inverted data output
61	GND	Module Ground
62	RX8-	Receiver inverted data output
63	RX8+	Receiver non-inverted data output
64	GND	Module Ground
65	NC	NO Connect
66	Reserved	For future use
67	VCCTx1	+3.3V Power Supply
68	VCC2	+3.3V Power Supply
69	Reserved	For future use
70	GND	Module Ground
71	Tx7+	Transmitter non-inverted data input
72	Tx7-	Transmitter inverted data input
73	GND	Module Ground

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74	Tx5+	Transmitter non-inverted data input
75	Tx5-	Transmitter inverted data input
76	GND	Module Ground

Ordering Information

Part Number	Product Description
TSQS-854HG01-MC	QSFP-DD 400G SR8 100m@OM4 0°C ~ +70°C

References

1. QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER Rev 5.0
2. SFF-8665: “QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)”, Rev 1.9, June 29, 2015 and associated SFF documents referenced therein:
   i. SFF-8661
   ii. SFF-8679
   iii. SFF-8662
   iv. SFF-8663
   v. SFF-8672
   vi. SFF-8472
3. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011.
4. Common Management Interface Specification (CMIS) Rev 4.0.
5. IEEE P802.3bs, 400GAUI-8 Interface.
6. IEEE P802.3cm.

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